Cluster Tool Simulation and Analysis: Implant Source Life and Lot Scheduling

Cluster Tool Analysis Group

Macarena Palominos
Muhaimeinul Khan
Tariq Hanif
Luis Ayala

George Mason University
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1 Executive Summary

This document is a proposal by Cluster Tool Analysis Group (CTAG) to develop a Colored Petri Net (CPN) model to study and analyze the scheduling of lots to Implant tools, taking into account the life time of Implant ion sources. Section 2.1 provides the background information about the Implant process and source degeneration. Section 2.2 describes the problem to be solved. Section 3 presents the preliminary requirements for this project. Section 4 describes the approach that CTAG will take to tackle the problem. Section 5 describes the expected results of this project. Finally, Section 6 covers the project plan.

2 Problem Definition

2.1 Background

Cluster tools are systems used in the semiconductor processing industry to fabricate microelectronic devices and components. One of the advantages of cluster tools is that they can perform processes in sequences to improve product yield. All semiconductor processes depend on these tools to process wafers in their respective areas.

One such cluster tool, known as an implant tool, will be of interest for this study. Implant tools are composed of several hardware components with the main internal component being the ion source. The ion source is composed of two main components: a cathode and a filament. The filament heats up the cathode, which in turn interacts with the gas flow; thus, creating a plasma. The plasma is then guided through magnets, acting as ion filters, and is then accelerated to implant the filtered ions onto the surface of the wafers. The activities undertaken in this implant area will be the focus of this project.

In this area wafers are bombarded with ions from different elements in order to introduce dopants such as, Boron (B), Phosphorous (P), Arsenic (Ar), Carbon (C), and Germanium (Ge) into and on top of the wafer to modify its conductivity. The specific format used to implant these elements is known as the implantation recipe.

This recipe is critical in helping to optimize the throughput of implant tools, which has gained great interest today as semiconductors are reducing in size. One method in particular used to improve product yield is Recipe Sequencing. This method can reduce the tool preparation time between different implantation recipes by organizing the recipes in sequences, where the wafer batches are scheduled to be processed depending on the implantation recipe they require, instead of a first come, first serve basis.

2.2 Problem statement (SOW)

In the Implant tools, the interactions between the gases, the heated cathode and filament, and the plasma, affect the thickness of the source's cathode. Certain gases, such as Boron (B), deposit or grow layers of substances on the surface of the cathode; other gases, such as Arsenic (Ar), Phosphorous (P), Carbon (C), and Germanium (Ge), tend to erode the surface of the cathode, making it thinner. Thus, running a process with the same element for too long may lead to failure of the ion source.

If the cathode of the source component becomes too thin, the plasma may have direct contact with the source's filament, leading to source failure. Similarly, if there is too much build up on the surface of the source's cathode, the uniformity of the ion beam is deteriorated, leading to defects on the implanted wafer. On both situations, the source needs to be replaced, which introduces delays between implantations.

Current recipe sequencing doesn't take source deterioration into account, which results in frequent source changes and a potentially less than optimal throughput. Therefore, there's a need for analysis of recipe sequencing on source degeneration. If the source's lifetime could be extended by utilizing a specific recipe schedule, unnecessary delays could be prevented, and the throughput may be improved.

2.3 Scope

In this project, the CTAG will look at one Implant tool to explore the improvement opportunities for recipe sequencing. Moreover, the areas of interest are:

- The effect of different recipe sequences on time to completion for Lot processing
- The effect of different recipe sequences on the thickness of the cathode's surface
- The effect of considering the thickness of the cathode's surface on recipe scheduling

3 Preliminary Requirements

3.1 Cluster Tool Analysis Group Requirements

Our objective is to provide our sponsor with an analysis of Implant recipe sequencing and recommend solutions to improve processing times and efficiency. In order to accomplish that goal, we will create appropriate process models, and provide Micron Technologies with our analysis and recommendations.

1) The GMU team shall use an architecture framework to develop appropriate architecture viewpoints.
2) The GMU team shall use CPN Tools (www.cpntools.org) to develop an executable model(s) for Implant recipe sequence processing.
3) The GMU team shall perform analysis on Implant recipe sequence processes.
4) The GMU team shall produce monthly informal progress reports for sponsor to show project progress
5) The GMU team shall produce a final report to be presented to the stakeholders on December 7th 2012.
6) The GMU team shall produce a website containing the final report and presentation.

3.2 Sponsor Requirements

1) Sponsor shall provide appropriate data to the GMU team for Implant tool simulation and analysis of recipe sequencing

4 Approach

4.1 Architecture Framework

There are many architecture development frameworks available. Therefore, one that relates to the semiconductor area must be selected. Current frameworks being considered are:

- Department of Defense Architecture Framework (DODAF)
- Joint Technical Architecture Framework (JTAF)
- The Open Group Architectural Framework (TOGAF)
- Automotive Architecture Framework (AAF)

A combination of frameworks is possible. The most important product from the architecture framework will be a class diagram, which will be used in the development of the executable model.

4.2 Executable Model

Colored Petri Nets (CPN) will be used in the development of the simulation model(s) for the following reasons:

a) The existence of a methodology for converting class diagrams into CPN models
b) Short time for model development
c) Highly visual development that aids in the understanding of model operation
d) Ability to use with data management software, such as Microsoft excel, for model analysis

4.3 Mathematical Analysis

Many mathematical analysis techniques and methods are available for data analysis. Therefore the Cluster tool analysis group (CTAG) will research and identify the method(s) that are applicable to the semiconductor area. Some techniques under consideration are:

- Dynamic Programming
- Linear Programming
- Shortest path heuristics
- State space analysis

A combination of more than one method or technique is possible.

4.4 Validation & Verification of analysis

After the CPN model has been developed and mathematical analysis has been performed. The possible suggestions for improvement will be validated and verified through the CPN model.

5 Expected Results

5.1 Objectives

The expected outcomes of this project are:

5.1.1 Develop a systems engineering approach to cluster tool analysis through the use of Architectural Frameworks

5.1.2 Develop a Colored Petri Net (CPN) model that runs recipe sequences for one Implant tool

5.1.3 Identification of recipe sequencing for Implant Tools based on ion source deterioration in order to improve ion source life and Implant tool performance

5.2 Success Criteria

The CTAG will consider the project to be successful when objectives 5.1.1, 5.1.2, and 5.1.3 have been achieved.

6 Project Plan

6.1 WBS

The following figure depicts a tree structure view of the breakdown of project tasks.

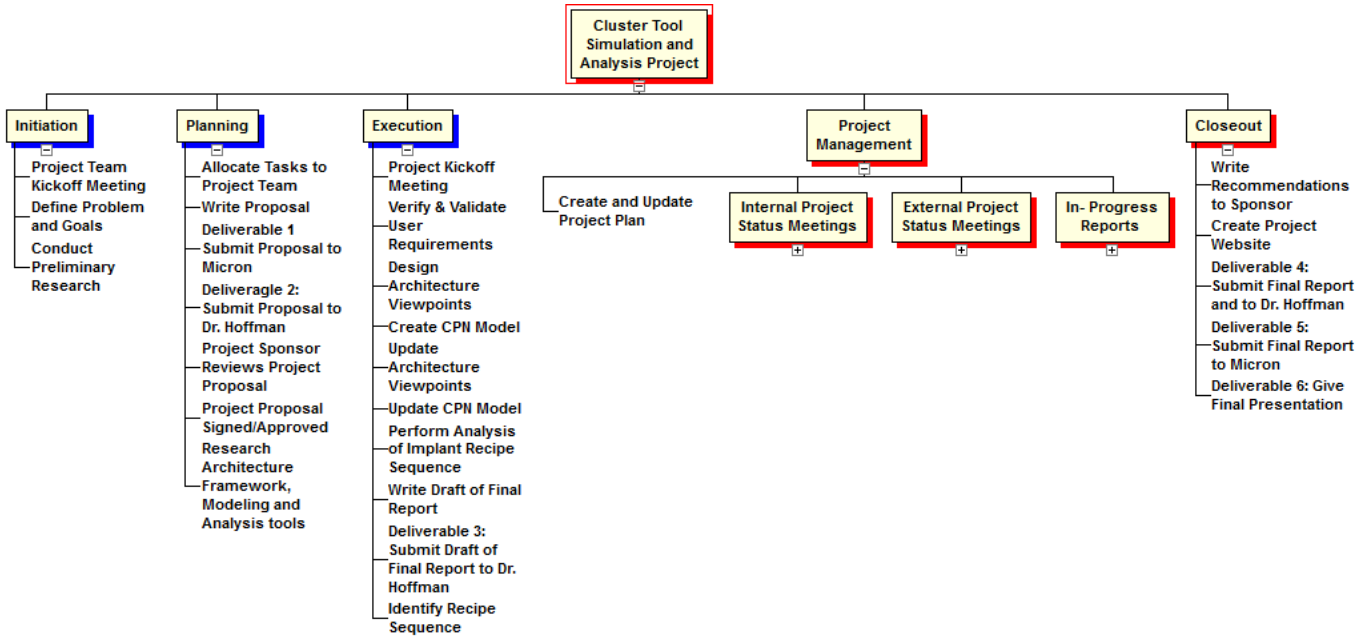

Figure 1: WBS Chart

6.2 Schedule

The following Gantt chart shows the breakdown of tasks with their durations on the left, and the schedule on the right.

ID	Task Name	Start	Finish	Duration
1	**Cluster Tool Simulation and Analysis Project**	**Thu 8/30/12**	**Fri 12/7/12**	**74 days**
2	**Initiation**	**Thu 8/30/12**	**Wed 9/5/12**	**5 days**
6	**Planning**	**Thu 9/6/12**	**Tue 9/18/12**	**10 days**
14	**Project Management**	**Thu 9/6/12**	**Thu 12/6/12**	**68 days**
42	**Execution**	**Tue 9/18/12**	**Fri 11/30/12**	**55 days**
43	Project Kickoff Meeting	Mon 9/17/12	Mon 9/17/12	0 days
44	Verify & Validate User Requirements	Mon 9/17/12	Thu 9/20/12	4 days
45	Design Architecture Viewpoints	Mon 9/17/12	Fri 10/5/12	15 days
46	Create CPN Model	Wed 10/3/12	Fri 10/19/12	13 days
47	Update Architecture Viewpoints	Mon 10/8/12	Fri 10/26/12	15 days
48	Update CPN Model	Wed 10/24/12	Fri 11/9/12	13 days
49	Perform Analysis of Implant Recipe Sequence	Mon 10/8/12	Fri 11/23/12	35 days
50	Write Draft of Final Report	Fri 10/26/12	Thu 11/1/12	5 days
51	*Deliverable 3: Submit Draft of Final Report to Dr. Hoffman*	*Thu 11/1/12*	*Thu 11/1/12*	*0 days*
52	Identify Recipe Sequence	Sat 11/24/12	Sat 11/24/12	1 day
53	**Closeout**	**Mon 11/26/12**	**Fri 12/7/12**	**10 days**
54	Write Recommendations to Sponsor	Mon 11/26/12	Fri 11/30/12	5 days
55	Create Project Website	Mon 12/3/12	Fri 12/7/12	5 days
56	*Deliverable 4: Submit Final Report and to Dr. Hoffman*	*Thu 11/29/12*	*Thu 11/29/12*	*0 days*
57	*Deliverable 5: Submit Final Report to Micron*	*Fri 11/30/12*	*Fri 11/30/12*	*0 days*

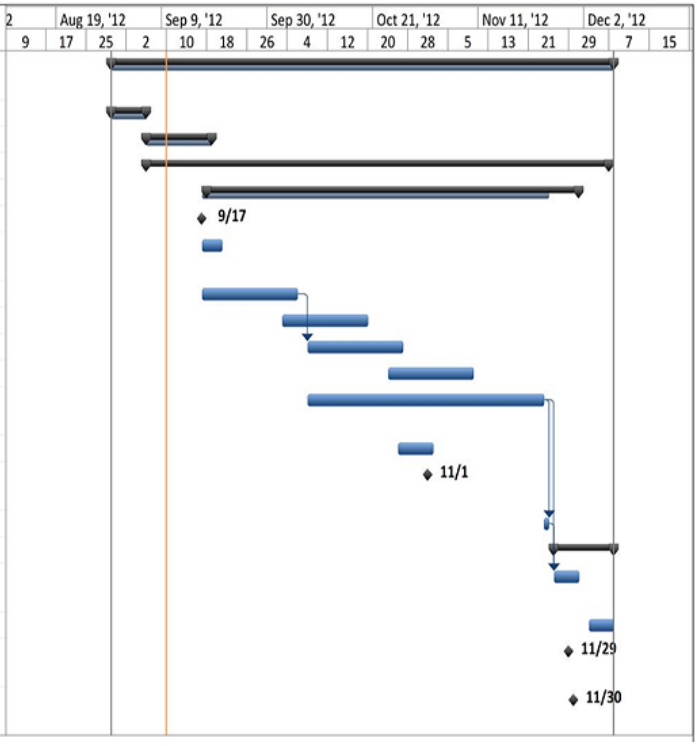

Figure 2: Project Schedule

6.3 Deliverables

Date	Deliverable
9/6/12	Problem Definition Presentation
9/13/12	Project Proposal Document
9/27/12	In-Progress Report 1 Document & Presentation
9/28/12	Monthly Informal Progress report for Sponsor
10/11/12	In-Progress Report 2 Document & Presentation
10/18/12	In-Progress Review Presentation
10/26/12	Monthly Informal Progress report for Sponsor
11/1/12	Draft of Final Presentation
11/29/12	Dry Run of Final Presentation
11/29/12	Final Report Document
11/30/12	Monthly Informal Progress report for Sponsor
12/7/12	Final Presentation

6.4 References

6.4.1 Systems Architecture

DOD Architectural Framework v2.02. *Chief Information Officer U.S. Department of Defense.* (n.d.). U.S. Department of Defense. Retrieved 10 September 2012.<http://dodcio.defense.gov/dodaf20.aspx>

Department of Defense Joint Technical Architecture Framework volume 1. *Office of the Under Secretary of Defense for Acquisition, Technology, and Logistics.* 3 October 2003. U.S. Department of Defense. Retrieved 10 September 2012.<http://www.acq.osd.mil/osjtf/pdf/jta-vol-I.pdf>

Welcome to TOGAF v9.1, an Open Standard. *The Open Group.* (n.d.). The Open Group. Retrieved 10 September 2012. <http://pubs.opengroup.org/architecture/togaf9-doc/arch/>

Dandashi, Fatima; Blevins, Terence; Siegers, Rolf; Jones, Judith. "So Many Frameworks…So Little Time: What's An Architect To Do?" *SOA Magazine*. 7 February 2007. Retrieved 10 September 2012. < http://soa.sys-con.com/node/329849>

Feng Ni; Ming-Zhe Wang ; Jing-Jing Liao ; Jing-Dan Zhou ; , "Enhancing DODAF with a HCPN Executable Model to support Validation," Computational Intelligence and Design, 2009. ISCID '09. Second International Symposium on, (2009): 283-287. IEEE Xplore. Web.

6.4.2 Process Modeling

Zuberek, W.M.; , "Cluster tools with chamber revisiting-modeling and analysis using timed Petri nets," *Semiconductor Manufacturing, IEEE Transactions on* 17.3 (2004): 333-334. IEEE Xplore. Web.

Naiqi Wu; Chengbin Chu; Feng Chu; Meng Chu Zhou; , "A Petri Net Method for Schedulability and Scheduling Problems in Single-Arm Cluster Tools With Wafer Residency Time Constraints," *Semiconductor Manufacturing, IEEE Transactions on* , 21.2 (2008): 224-237. IEEE Xplore. Web.

H.-Y. Lee and T.-E. Lee "Scheduling single-armed cluster tools with reentrant wafer flows", *IEEE Trans. Semicond. Manuf.*, 19.2 (2006): 226-240. IEEE Xplore. Web.

Dimmler, M.A. "Using simulation and genetic algorithms to improve cluster tool performance," *Simulation Conference Proceedings,* 1 (1999):875-879. IEEE Xplore. Web.

Poolsup, S.; Deshpande, S. "Cluster tool simulation assists the system design," *Simulation Conference, 2000,* 2 (2000): 1443-1448. IEEE Xplore. Web.

Srinivasan, R.S. "Modeling and performance analysis of cluster tools using Petri nets" *Semiconductor Manufacturing, IEEE Transactions on* , 11 (1998): 394-403. IEEE Xplore. Web.

Han-Pang Huang; Che-Lung Wang; "The modeling and control of the cluster tool in semiconductor fabrication," *IEEE International Conference on Robotics and Automation. Proceedings 2001 ICRA. IEEE,* 2 (2001): 1826- 1831. IEEE Xplore. Web.

6.4.3 Mathematical Analysis

Wood, S.C.; Tripathi, S.; Moghadam, F.; , "A generic model for cluster tool throughput time and capacity," *Advanced Semiconductor Manufacturing Conference and*

Workshop. 1994. ASMC 94 Proceedings. IEEE/SEMI . (1994): 194-199. IEEE Xplore. Web.

Chihyun Jung; Tae-Eog Lee; , "An Efficient Mixed Integer Programming Model Based on Timed Petri Nets for Diverse Complex Cluster Tool Scheduling Problems," *Semiconductor Manufacturing, IEEE Transactions on*. 25.2 (2012): 186-199. IEEE Xplore. Web.

Dae-Kyu Kim; Yu-Ju Jung; Chihyun Jung; Tae-Eog Lee; , "Cyclic Scheduling of Cluster Tools With Nonidentical Chamber Access Times Between Parallel Chambers," *Semiconductor Manufacturing, IEEE Transactions on*. 25.3 (2012): 420-431. IEEE Xplore. Web.

Shengwei Ding; Jingang Yi; Zhang, M.T.; , "Multicluster tools scheduling: an integrated event graph and network model approach," *Semiconductor Manufacturing, IEEE Transactions on*. 19.3 (2006): 339-351. IEEE Xplore. Web.

Liangliang Sun; Luh, P.B.; Shian-Ching Chiou; Shi-Chung Chang; Jen-Hsuan Ho; Hsin Yuan Chen; Ji-Lun Chen; Chang, J.; Hsu, S.; , "Efficient dual-armed cluster tool performance via branch and cut optimization algorithm," *Intelligent Control and Automation (WCICA), 2011 9th World Congress on*. (2011): 79-84. IEEE Xplore. Web.

J.-H. Paek and T.-E. Lee "Optimal scheduling of dual-armed cluster tools without swap restriction", *Proc. IEEE Conf. Automat. Sci. Eng.* (2008): 103 -108. IEEE Xplore. Web.

Chihyun Jung; Tae-Eog Lee "An Efficient Mixed Integer Programming Model Based on Timed Petri Nets for Diverse Complex Cluster Tool Scheduling Problems," *Semiconductor Manufacturing, IEEE Transactions on* , 25.2 (2012): 186-199. IEEE Xplore. Web.